What is claimed is:

1. A method of creating a copper interconnect, comprising:

providing a substrate, semiconductors having been provided in or over the substrate, at least one contact point of first level copper having been provided in or over the substrate;

creating at least one interconnect opening through layers of semiconductor material over the substrate aligned with the at least one contact point;

filling the at least one interconnect opening with copper after sidewalls of the at least one interconnect opening have been lined with a doped copper seed layer, creating at least one copper interconnect;

applying an anneal to the copper in the at least one interconnect opening and the doped copper seed layer;

depositing an oxide based layer over the layers of semiconductor material and the at least one copper interconnect; and

depositing a cap layer over the oxide based layer.

2. The method of claim 1, the layers of semiconductor material comprising at least one layer of etch stop material and at least one layer of low-k dielectric.

3. The method of claim 1, additionally lining sidewalls of the at least one interconnect opening with a layer of barrier material prior to lining sidewalls of the at least one interconnect opening with the doped copper seed layer.

4. The method of claim 1, wherein a profile of the at least one interconnect opening is a single damascene profile, a dual damascene profile, a contact opening profile or a via opening profile.

5. The method of claim 1, the oxide based layer comprising silicon oxide, deposited to a thickness between about 50 and 300 Angstrom.

6. A method for the creation of a copper interconnect, comprising:

providing a substrate, semiconductors having been provided in or over the substrate, at least one contact point of first level copper having been provided in or over the substrate;

creating at least one interconnect opening through layers of semiconductor material over the substrate aligned with the at least one contact point;

depositing a doped copper seed layer over the layers of semiconductor material, including inside surfaces of the at least one interconnect opening;

depositing a layer of copper over the doped copper seed layer, filling the at least one interconnect opening;

applying an anneal to the substrate and thereover created layers;

removing excess copper and the seed layer from the layers of semiconductor material, creating at least one copper interconnect;

depositing an oxide based layer over the layers of semiconductor material, including the at least one copper interconnect; and

depositing a cap layer over the oxide based layer.

7. The method of claim 6, additionally depositing a layer of barrier material over the layers of semiconductor material, including inside surfaces of the at least one interconnect opening, prior to the depositing a doped copper seed layer.

8. The method of claim 7, wherein the layer of barrier material is Ta, TaN or TiN.

9. The method of claim 7, the layer of barrier material being deposited to a thickness between about 50 and 300 Angstrom.

10. The method of claim 6, the layers of semiconductor material comprising at least one layer of etch stop material and at least one layer of low-k dielectric.

11. The method of claim 6, the doped copper seed layer comprising a doping element selected from the group consisting of Cr, Pd, Sn, Ti, Zr, Mg, Al.

12. The method of claim 6, the doped copper seed layer being deposited to a thickness between about 50 and 300 Angstrom.

13. The method of claim 6, the anneal comprising applying about 400 degrees C applied for about 2 minutes.

14. The method of claim 6, the removing excess copper comprising methods of Chemical Mechanical Polishing or surface etch.

15. The method of claim 6, the depositing an oxide based layer comprising a plasma enhanced CVD (PECVD) of oxide to a thickness between about 50 and 300 Angstrom.

16. The method of claim 6, the etch stop layer comprising a material selected from the group consisting of SiN and SiC and SiCN.

17. The method of claim 6, the oxide based layer comprising silicon oxide.

18. The method of claim 6, wherein a profile of the at least one interconnect opening is a single damascene profile, a dual damascene profile, a contact opening profile or a via opening profile.

19. An copper interconnect having improved adhesion, comprising:

a substrate comprising semiconductors in or over the surface there-of, further comprising at least one contact point of first level copper;

at least one interconnect opening through layers of semiconductor material over the substrate aligned with the at least one contact point;

at least one annealed copper interconnect comprising:

(i) doped copper seed layer over inside surfaces of the at least one interconnect opening; and

(ii) a layer of copper over the doped copper seed layer, filling the at least one interconnect opening;

an oxide based layer over the layers of semiconductor material, including the at least one annealed copper interconnect; and

a cap layer over the oxide based layer.

20. The copper interconnect of claim 19, additionally comprising underlying the doped copper seed layer a layer of barrier material over inside surfaces of the at least one interconnect opening.

21. The copper interconnect of claim 20, wherein the layer of barrier material is Ta, TaN or TiN.

22. The copper interconnect of claim 20, the layer of barrier material having a thickness between about 50 and 300 Angstrom.

23. The copper interconnect of claim 19, the layers of semiconductor material comprising at least one layer of etch stop material and at least one layer of low-k dielectric.

24. The copper interconnect of claim 19, the doped copper seed layer comprising a doping element selected from the group consisting of Cr, Pd, Sn, Ti, Zr, Mg, Al.

25. The copper interconnect of claim 19, the doped copper seed layer being deposited to a thickness between about 50 and 300 Angstrom.

26. The copper interconnect of claim 19, the oxide based layer having a thickness between about 50 and 300 Angstrom.

27. The copper interconnect of claim 19, wherein the etch stop layer is SiN, SiC or SiCN.

28. The copper interconnect of claim 19, the oxide based layer comprising silicon oxide.

29. The copper interconnect of claim 19, wherein a profile of the at least one interconnect opening is a single damascene profile, a dual damascene profile, a contact opening profile or a via opening profile.

30. The method of claim 1, wherein the cap layer is an etch stop material.

31. The method of claim 6, wherein the cap layer is an etch stop material.

32. The method of claim 19, wherein the cap layer is an etch stop material.